6G-RIC
Research and
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GEFÖRDERT VOM
Bundesministerium
für Bildung
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Heterointegration of InP-Chiplets on BiCMOS for D-Band Transceivers

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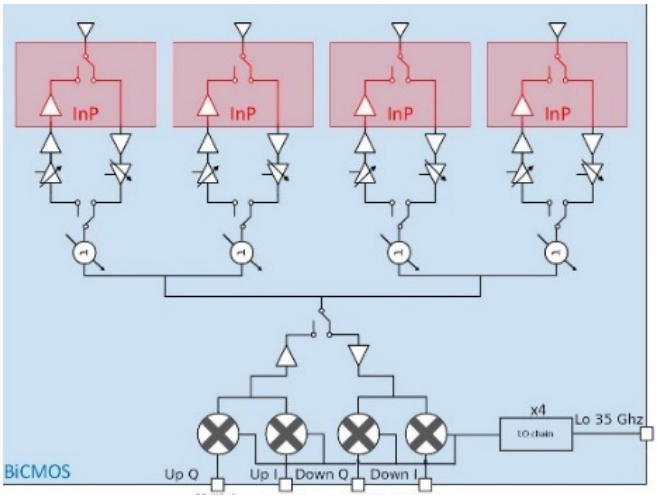
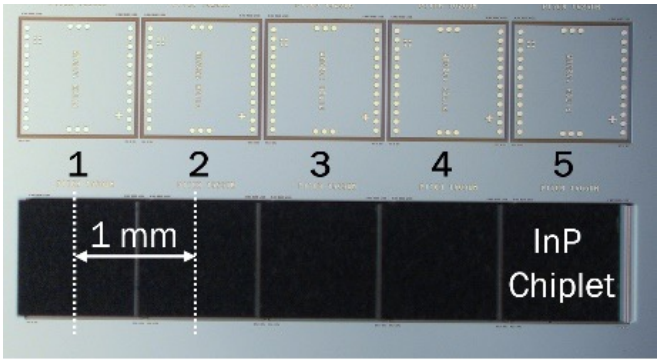
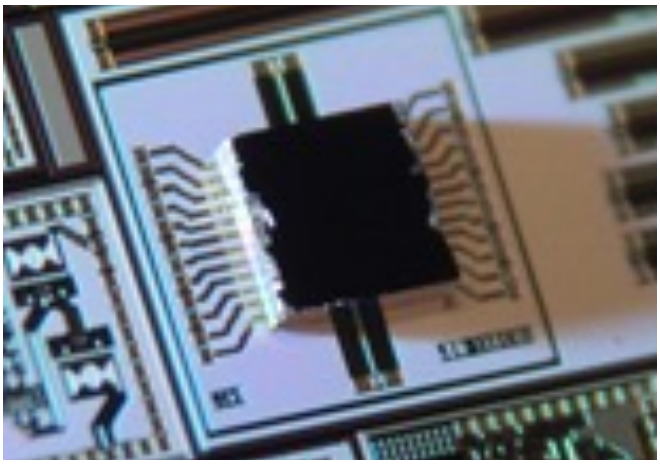
Boost RF transceiver performance at D-band with regard to output power and energy efficiency, by means of InP-on-BiCMOS heterointegration. The approach has to be compatible with typical microelectronic processing and should be scalable to allow for multi-channel realizations.



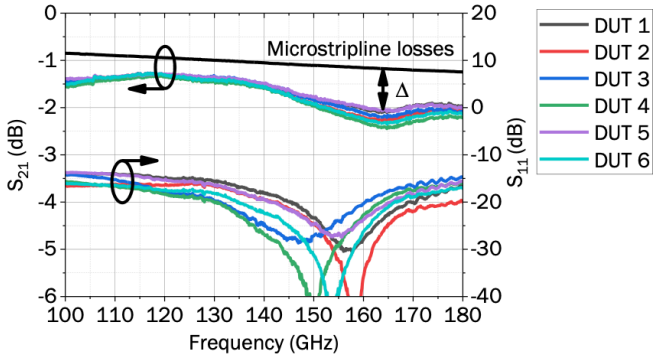
a) The idea: 4-channel transceiver (block diagram) combining InP HBT and BiCMOS



b) Test of scalability: 5 InP chiplets mounted next to each other with only 1 mm pitch with a chip width of 950 µm, as needed for multi-channel transceivers



c) The experimental status: W-band InP PA on a BiCMOS wafer



d) Small signal measurements of 6 individual flip-chip bonded InP-Chiplets on a BiCMOS Chip. Δ indicates the additional loss caused by two RF-flip-chip-interconnects, which is very low (< 0.5 dB per interconnect).

The block diagram a) illustrates how the InP chiplets (red) are to complement the BiCMOS transceiver. The PA and the antenna switch will be realized as InP HBT circuits, to allow for higher output power and efficiency, while the remaining TRX functions will be on BiCMOS. For MIMO realizations in D-band array pitch requires to place chiplets in a row with narrow spacing (see Fig. b)). Fig. c) presents the status so far: An InP-on-BiCMOS assembly with a single InP PA chiplet at 90 GHz. D-band performance (insertion loss <0.5 dB per interconnect) and reproducibility are shown in graph d).

KEY FINDINGS

The research work involves four main tasks:

- Advance bipolar InP process for operation in D-band by suitable downscaling of the transistor node from 850 nm to 400 nm.
- Develop PA and antenna switch as chiplet in InP HBT technology
- Provide BiCMOS-based transceivers to be combined with the InP circuit part
- Integrate the InP chiplets with the SiGe-BiCMOS chip accounting for wideband interconnects, reliability and multi-channel scalability

Downscaling the transistor node to 400 nm is in progress. At the same time, HBT geometry, epitaxy and processing has been optimized to improve fmax and fT. For a 500 nm node, an fmax of ca. 400 GHz has been achieved, which allows for reasonable power gain within the complete D band. While circuit development in D-band is still in progress, the integration approach has already reached a mature state: Miniaturized indium bumps are used as interconnects, their soldering temperature is compatible with the thermal restrictions of the InP HBT devices. With InP test chiplets on a BiCMOS passive chip an impressive wideband features of the InP-on-BiCMOS assembly was obtained, with excellent reproducibility: A bandwidth from DC up to more than 300 GHz with merely 0.5 dB insertion loss per interconnect. This demonstrates the excellent RF performance of the hetero-integration approach.

H. Yacoub et al., "Heterointegration of mm-Wave InP-HBT Power Amplifier Chiplets on SiGe-BiCMOS Chip," 2023 18th European Microwave Integrated Circuits Conference (EuMIC), Berlin, Germany, 2023, pp. 169-172

M. Rausch et al., "Broadband Hetero-Integration of InP Chiplets on SiGe BiCMOS for mm-Wave MMICs up to 325GHz," 2023 IEEE/MTT-S International Microwave Symposium - IMS 2023, San Diego, CA, USA, 2023, pp. 466-469